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ISL97645A Evaluation Board Application Manual

Description

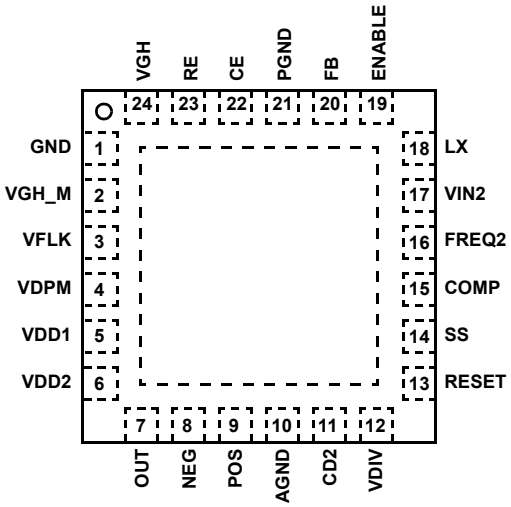
The ISL97645A EVB is an evaluation board for the ISL97645A, a DC/DC voltage regulator for TFT-LCD displays with screen sizes up to 20". ISL97645A integrates a boost converter, a V_{ON} slice circuit, a supply monitor circuit and a high performance V_{COM} amplifier. This evaluation board is designed to:

1. Deliver up to 0.8A current for AVDD supply to the source / column driver ICs.
2. Generate different V_{ON} (gate high) and V_{OFF} (gate low)
3. Modulated VGH_M output for gate high voltage with desired delay time and discharging slope using the V_{ON} slice circuit
4. The high performance amplifier generates the LCD pixel common bias voltage (VCOM)
5. Generate a RESET signal correctly at power on and off

The ISL97645A evaluation board provides a dip switch that allows users to select either 650kHz or 1.2MHz and the enable signal to enable or disable the IC.

Pinout

ISL97645A
(24 LD 4x4 QFN)
TOP VIEW



Features

- A complete TFT-LCD PMIC evaluation platform for the ISL97645A
- Input voltage: 2.7V to 5.5V
- Non-synchronous boost for AVDD supply
- V_{ON} and V_{OFF} charge pumps for gate driver IC supplies
- V_{ON} slice circuit for VGH_M
- Supply monitor circuit to generate the RESET signal
- Op Amp follower for VCOM
- Layout Guidelines
- RoHS compliant

What is Needed

- The following instruments will be needed to perform testing:
  - Power supplies
  - DC Electronic load
  - Multimeters
  - Oscilloscope
  - Resistors
  - Cables and wires

Ordering Information

PART #	DESCRIPTION
ISL97645AIRZ-EVALZ	Evaluation Board for ISL97645A

Quick Setup Guide

Step 1: Connect power supply between headers of VIN and VIN_GND. The positive output of the power supply should be connected to VIN header. Set power supply voltage between 2.7V and 5.5V, and current limit at 4A.

Step 2: Connect the positive and negative inputs of the Electronic load to AVDD header and AVDD_GND, respectively. The load current should not exceed the maximum output current in Table 1.

Step 3: Put S1 to the direction of the arrow to tie FREQ pin to VIN to set 1.2MHz switching frequency; put S1 to the reverse direction of the arrow to pull FREQ to ground with R16 to set 650kHz.

Step 4: Put S2 to the direction of the arrow to tie ENABLE pin to VIN to enable the part; put S2 to the reverse direction of the arrow to pull Enable to ground with R17 to disable the part.

Step 5: Connect VDIV to a resistive divider between headers of VIN and VIN_GND.

Step 6: Connect Electronic load between headers of V_{ON} and Vin_GND. The positive input of the E-load should be connected to V_{ON} header, the negative input of the E-load should be connected to Vin_GND. Connect E-load between headers of V_{OFF} and Vin_GND. The positive input of the E-load should be connected to Vin_GND header, the negative input of the E-load should be connected to V_{OFF}. Set current values of E-load. The values of V_{ON} and V_{OFF} at different loadings are shown in Table 2.

Step 7: Connect header of V_{ON} to VGH pin

Step 8: Connect input from signal generator between headers of VFLK and SGND. Select y to square waveform with an amplitude of 3.3V and frequency of 50kHz

Step 9: Connect power supply between headers of POS and SGND. Set power supply voltage at desired VCOM value.

Step 10: Make sure all the connections on the EVB are correct, then turn on power supply and E-loads. The part starts to operate.

Maximum Output Current

The MOSFET current limit is 2.6A. This limits the maximum output current that ISL97645A can drive. Table 1 shows the maximum output current I_{OMAX} at different input and output voltages.

TABLE 1. TYPICAL MAXIMUM OUTPUT CURRENT

V_{IN} (V)	V_{OUT} (V)	I_{OMAX} (mA)
3.3	8	800
3.3	12	480
5	8	1370
5	12	850

Notes:

1). Table 1 shows typical maximum output current values for 1.2MHz switching frequency and 10µH inductor.

2). Maximum current values in actual application may vary with component variance

3). Feedback compensation parameters, input and output capacitance of the boost may need to be modified to keep good stability with maximum peak inductor current of 2.6A.

Gate Pulse Modulator Timing Diagram

ISL97645A evaluation board can generate a modulated VGH_M with a fixed power on delay time, a discharging slope and a delay time to the falling edge of VFLK. The waveform of VGH_M is shown in Figure 1 and Figure 2.

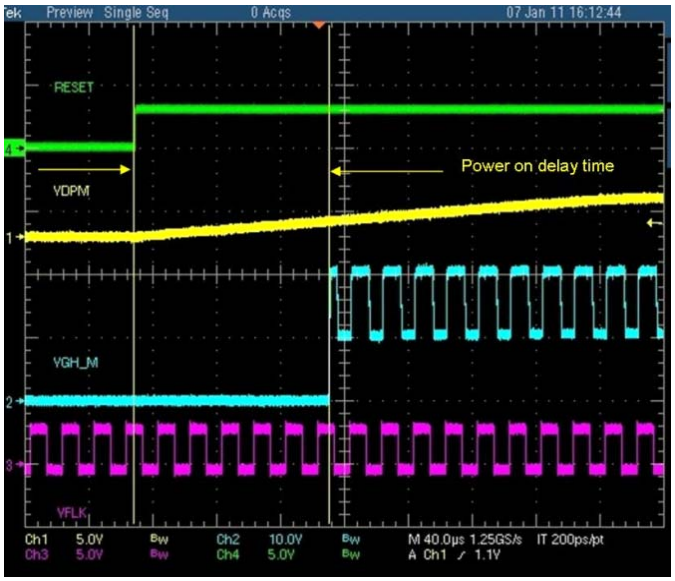


FIGURE 1. POWER ON DELAY TIME

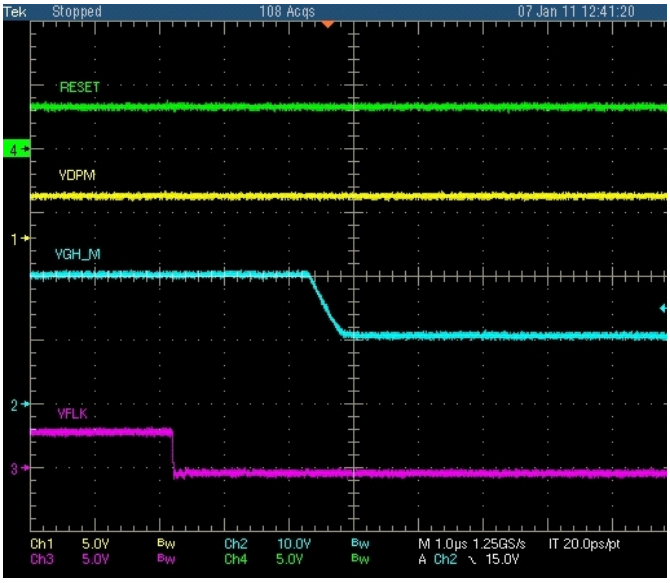


FIGURE 2. VGH_M

Supply Monitor Circuit

The supply monitor circuit monitors VDIV and sets open-drain output RESET low. When RESET changes to low and VGH is above 2.5V, VGH_M is pulled up to follow VGH until VGH falls below 2.5V. Figure 3 shows the RESET and VGH_M voltages at power off (when V_{IN} is dropping).

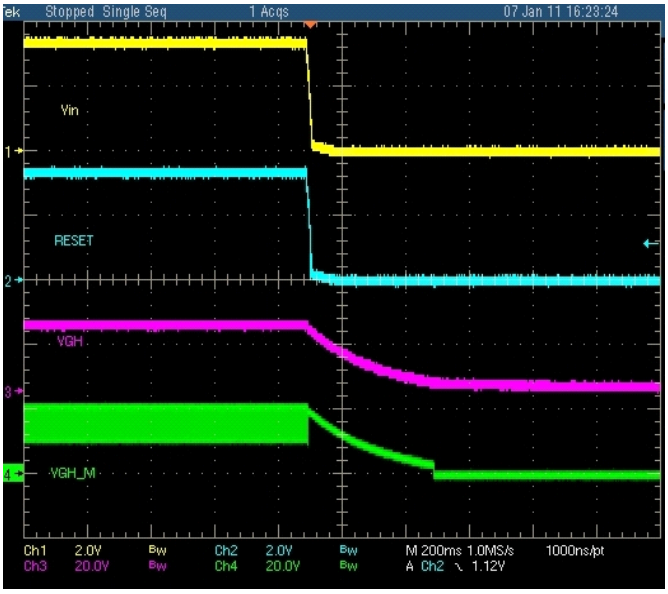


FIGURE 3. VGH_M IS PULLED TO VGH AT POWER OFF

VON and VOFF at Different Loadings

The boost converter integrated in ISL97645A is capable to output up to 20V AVDD. This ISL97645A EVA board generates VON and VOFF based on the output AVDD designed. Table 2 shows different values of VON and VOFF at different AVDD and different loadings. By removing R18 and adding C24 and D3 into the circuit, the charge pump is able to deliver a VON higher than 2*AVDD.

Layout Recommendation

The device performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

Following are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} and VDD bypass capacitors close to the pins.
3. Reduce the loop area with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and should be placed to the IC and as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point at the exposed die plate, underneath the package.
6. The exposed die plate should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separated from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for control circuit.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

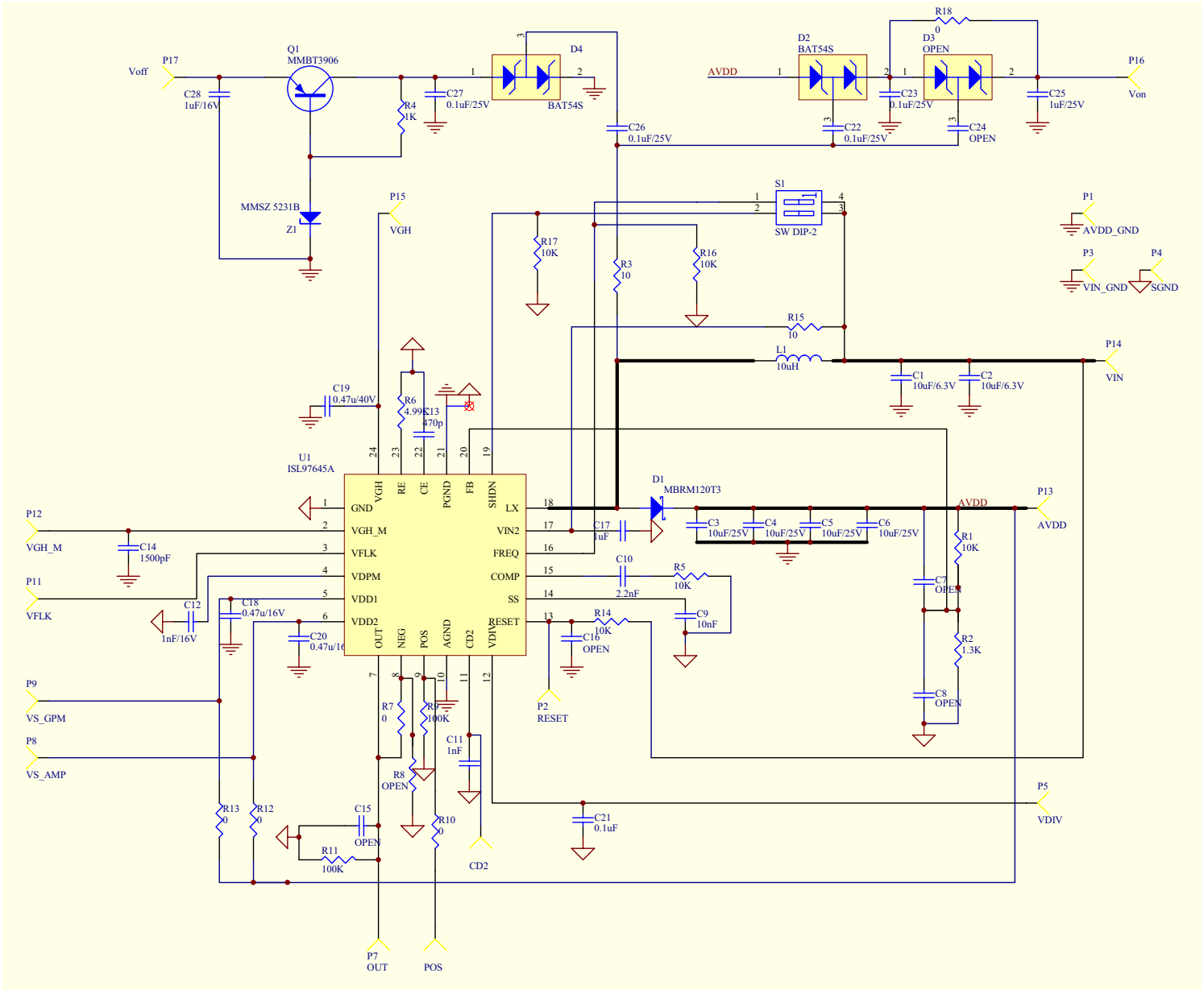
The EVB board layout on page 5 page 7 is available to illustrate the proper layout implementation.

TABLE 2. TYPICAL VON AND VOFF FOR DIFFERENT LOADINGS

	VON (V)				VOFF (V)		
ILOADING	AVDD = 8V Single Stage	AVDD = 8V Two Stages	AVDD = 10V	AVDD = 12V	AVDD = 8V	AVDD = 10V	AVDD = 12V
1mA	15.2	23.4	20.6	23.8	4.3	4.3	4.4
5mA	15.1	23.2	20.2	23.3	4.3	4.3	4.3
10mA	14.7	23.0	20.0	23.2	4.2	4.2	4.3

EVB Design

Schematic



EVB Layout

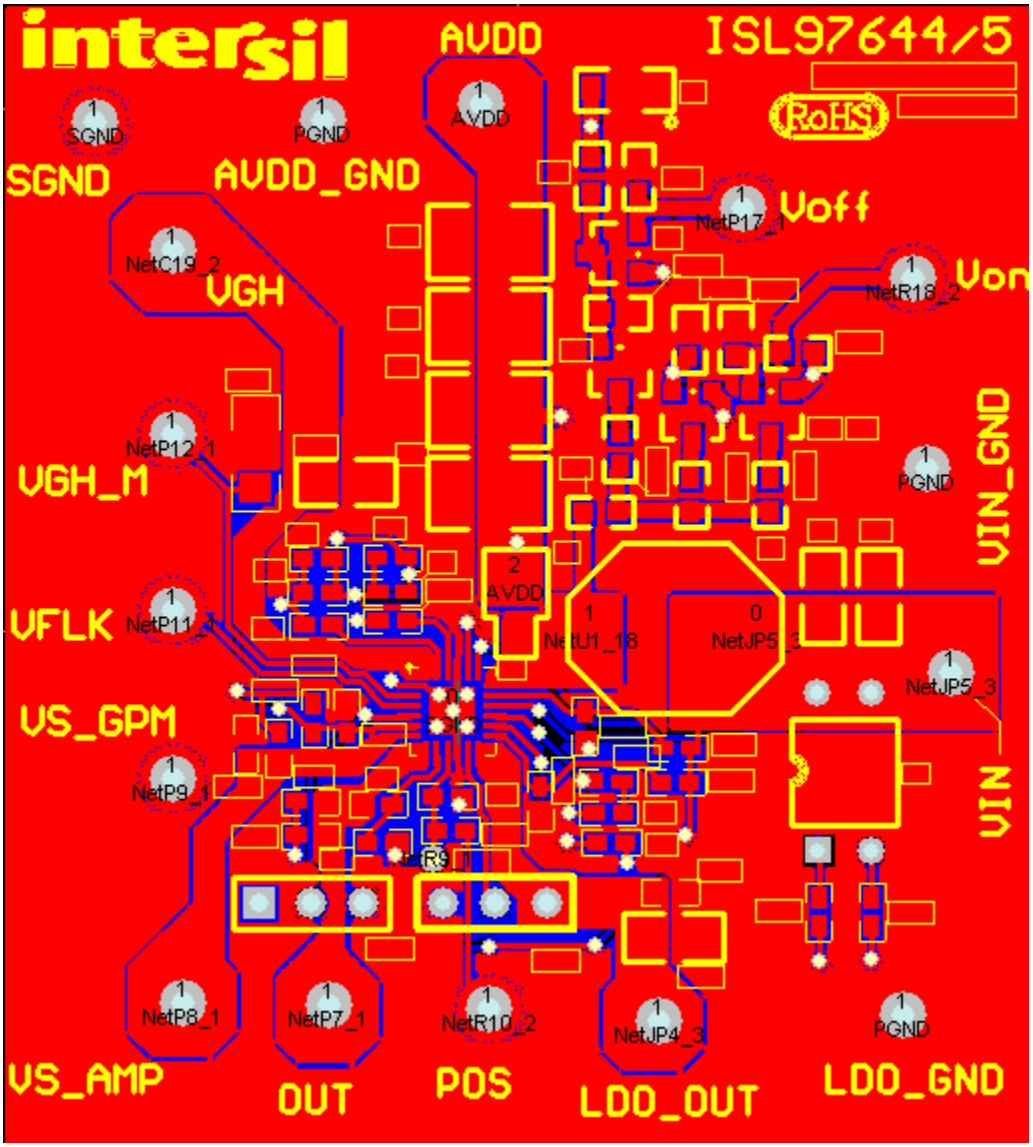


FIGURE 4. EVB ASSEMBLY LAYER

EVB Layout (Continued)

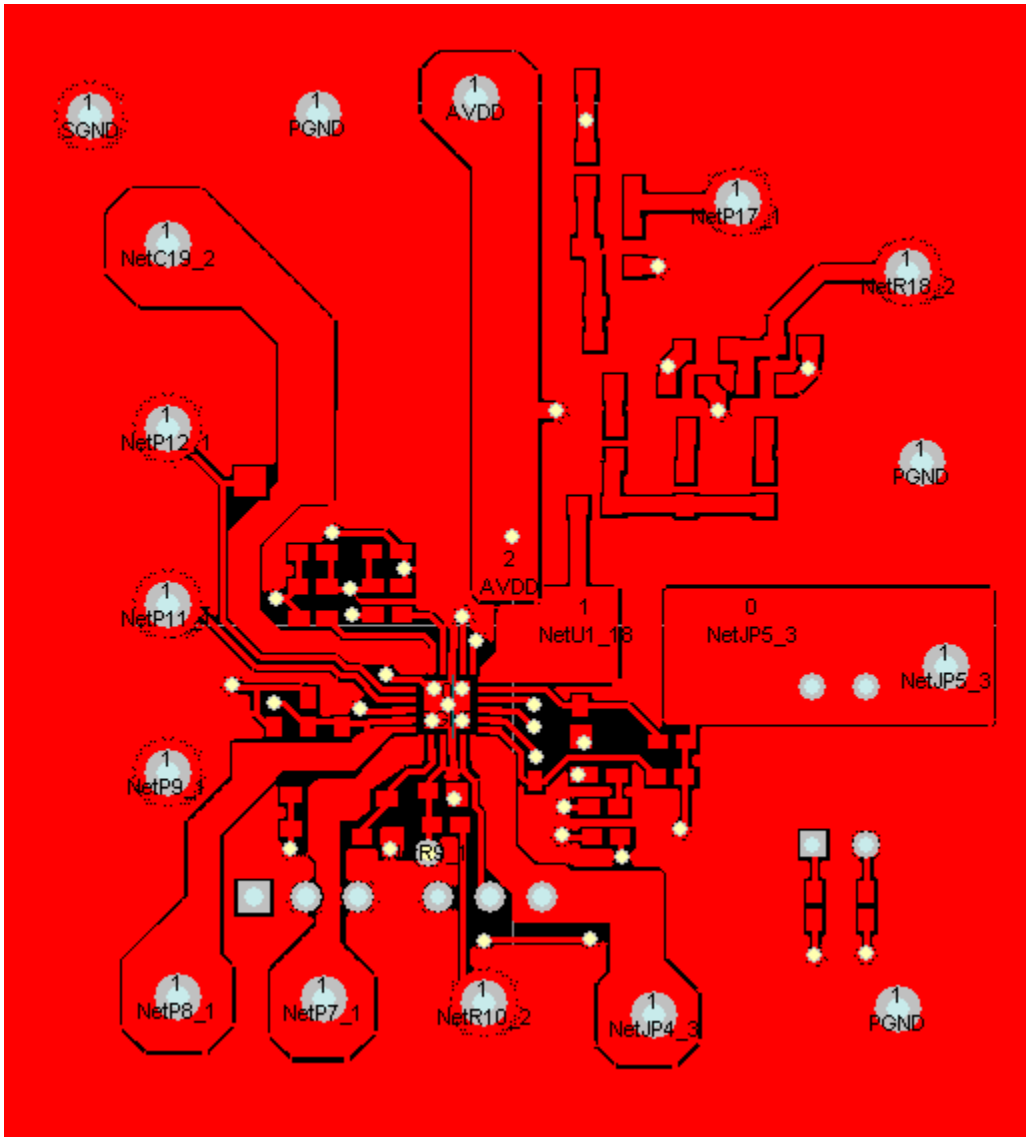


FIGURE 5. TOP LAYER

EVB Layout (Continued)

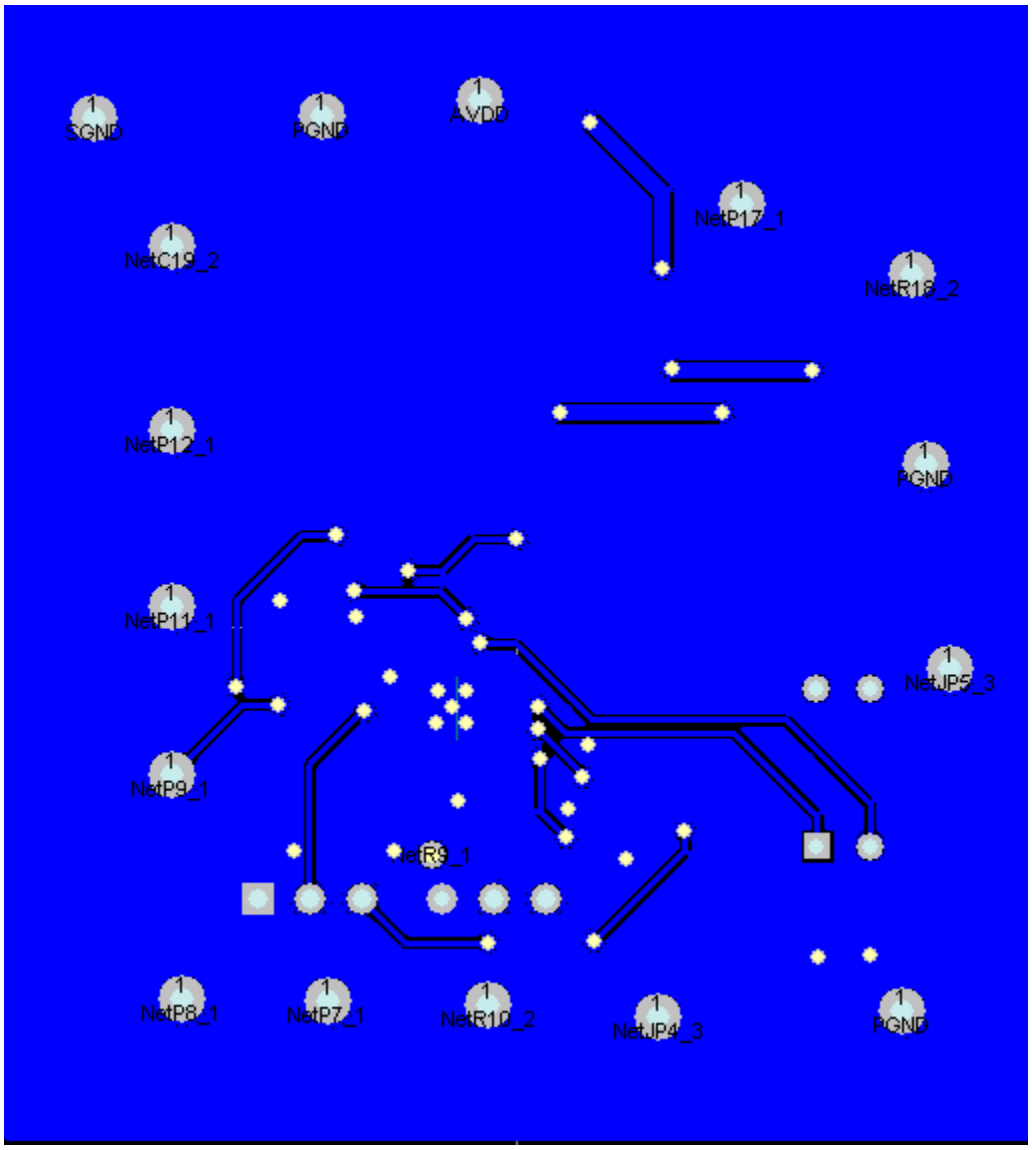


FIGURE 6. BOTTOM LAYER

BOM for ISL97645A Evaluation Board

PART TYPE	DESIGNATOR	FOOTPRINT
10k	R1	603
1.3k	R2	603
10	R3	603
1k	R4	603
10k	R5	603
4.99k	R6	603
0	R7	603
OPEN	R8	603
100k	R9	603
0	R10	603
100k	R11	603
0	R12	603
0	R13	603
10k	R14	603
10	R15	603
10k	R16	603
10k	R17	603
0	R18	805
10µF/6.3V	C1	805
10µF/6.3V	C2	805
10µF/25V	C3	1210
10µF/25V	C4	1210
10µF/25V	C5	1210
10µF/25V	C6	1210
OPEN	C7	603
OPEN	C8	603
10nF	C9	603
2.2nF	C10	603
1nF	C11	603
1nF/16V	C12	603
470p	C13	603
1500pF	C14	1206
OPEN	C15	603
OPEN	C16	603
1uF	C17	603
0.47µF/16V	C18	603
0.47µF/16V	C19	805
0.47µF/16V	C20	603
0.1µF	C21	603

BOM for ISL97645A Evaluation Board (Continued)

PART TYPE	DESIGNATOR	FOOTPRINT
0.1µF/25V	C22	603
0.1µF/25V	C23	603
OPEN	C24	603
1µF/25V	C25	603
0.1µF/25V	C26	603
0.1µF/25V	C27	603
1µF/16V	C28	603
MBRM120T3	D1	Case475
BAT54S	D2	SOT-23
OPEN	D3	SOT-23
BAT54S	D4	SOT-23
10µH	L1	RLF7030
AVDD_GND	P1	POWERPOST
LDO_GND	P2	POWERPOST
VIN_GND	P3	POWERPOST
SGND	P4	POWERPOST
VDIV	P5	POWERPOST
POS	P6	POWERPOST
OUT	P7	POWERPOST
VS_AMP	P8	POWERPOST
VS_GPM	P9	POWERPOST
CD2	P10	POWERPOST
VFLK	P11	POWERPOST
VGH_M	P12	POWERPOST
AVDD	P13	POWERPOST
VIN	P14	POWERPOST
VGH	P15	POWERPOST
V_{ON}	P16	POWERPOST
V_{OFF}	P17	POWERPOST
MMBT3906	Q1	SOT-23
SW DIP-2	S1	DIP4
ISL97645A	U1	
MMSZ 5233B	Z1	SOD-123